** Each question carries 8 mark 3×8=24**

2. Explain CMOS process flow with detailed diagram?

3. Explain Lithography process in detail ?

4.What are the limitations associated with Domino CMOS

logic ? Explain the concept of charge sharing and measures

to solve it?

5. Describe the Gradual Channel Approximation and derieve

the drain current equation for both linear and saturation mode?

6.Give the four different representation of the CMOS tran-

Mission gate(TG)? Implement a 2 input multiplexer circuit

Using 2 CMOS TG? Implement a XOR function using 8 and

6 transistors CMOS TG separately?

**SCHOOL OF ENGINEERING AND TECHNOLOGY**

D.C. COURT JUNCTION, DIMAPUR

**END SEMESTER EXAMINATIONS, JUNE 2017**

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| --- | --- | --- | --- | --- | --- |
| **Course Code** | EC6T03 | **Semester** | VI | **Total** | 60 Marks |
| **Course Name** | VLSI | | | **Time** | 3 hrs |

**PART A. (Multiple choices question)**

**Each question carries 1 mark 1×10=10**

1. Addition of which metal along with Al reduces electromigration effect

a) Copper b) Chromium c) Titanium d) Tungsten

2. During electromigration atoms pile up in one end in microscopic structures forming

a) Voids b) Hillocks c) beads d) Targets

3.Precharge and evaluation phase in Dynamic CMOS is when

a) respectively b) respectively

c) respectively

d) respectively

4.During charge sharing when the intermediate node capacitance C2 is equal to output node capacitance C1, then output node voltage after charge sharing becomes

a) 0 b) 1 c) d)

5. Dynamic power dissipation of CMOS inverter is given as

a) b)

c) d)

6.In constant voltage scaling the doping densities are increased

by a factor of

a) b) S c) 2S d)

7. In terms of MOSFET capacitances the cut-off mode is

represented as

a)

b)

c)

d)

8. When power supply voltage is reduced below

the VTC will

a ) Follow hysteresis b) Follow sharp VTC

c) Follow practical VTC curve d) Follow no path

9. Condition for Saturation in MOSFET operation is

a) b)

c) d)

10. The condition for surface inversion is

a) b) c) d)

**PART B. (Answer any five of the following question)**

**Each question carries 4 marks 5×4=20**

1 Explain the Lightly doped drain (LDD) nFET fabrication process?

2. Why Silicon Diode is considered an important material in IC processing. Explain the CVD oxide process with proper diagram?

3.Realise Z=AB+(C+D)(E+F)+GH, using standard CMOS and domino CMOS?

4.Explain Elmore Delay from any RC tree network and take example of any 1 nodes and calculate its delay

5. Explain CMOS Ring Oscillator Circuit?

6.Explain the operating regions of the nMOS and pMOS transistors with the VTC graph of the CMOS inverter?

7.Explain Thermal oxide growth of silicon. What are clean rooms.?

**PART C. (Question No 1 is compulsory.**

**Answer any three questions from the rest)**

**Question carries 6 marks 6×1 =6**

1.Draw the ckt diagram of the equation using CMOS. Draw the layout diagram and stick diagram?