Each question carries 8 mark **3×8=24**

2. Explain CMOS process flow with detailed diagram?

3. Explain Lithography process in detail ?

4. What are the limitations associated with Domino CMOS logic ? Explain the concept of charge sharing and measures to solve it?

5. Describe the Gradual Channel Approximation and derieve the drain current equation for both linear and saturation mode?

6.Give the four different representation of the CMOS tran-Mission gate(TG)? Implement a 2 input multiplexer circuit Using 2 CMOS TG? Implement a XOR function using 8 and 6 transistors CMOS TG separately?

SCHOOL OF ENGINEERING AND TECHNOLOGY

D.C. COURT JUNCTION, DIMAPUR

END SEMESTER EXAMINATIONS, JUNE 2017

Course Code	EC6T03	**Semester**	VI	**Total**	60 Marks
Course Name	VLSI			**Time**	3 hrs

PART A. (Multiple choices question)

Each question carries 1 mark **1×10=10**

1. Addition of which metal along with Al reduces electromigration effect

a) Copper b) Chromium c) Titanium d) Tungsten

2. During electromigration atoms pile up in one end in microscopic structures forming

a) Voids b) Hillocks c) beads d) Targets

3.Precharge and evaluation phase in Dynamic CMOS is when

a) $\varphi = 0\ and\ \varphi = -1$ respectively b) $\varphi = 1\ and\ \varphi = 0$ respectively
c) $\varphi = -1\ and\ \varphi = 0$ respectively
d) $\varphi = 0\ and\ \varphi = 1$ respectively

4.During charge sharing when the intermediate node capacitance C_2 is equal to output node capacitance C_1, then output node voltage after charge sharing becomes

a) 0 b) 1 c) $\frac{V_{DD}}{2}$ d) $\frac{V_{DD}}{4}$

5. Dynamic power dissipation of CMOS inverter is given as

a) $P_{avg} = C_{load}.V_{DD}^2.f$ b) $P_{avg} = C_{load}.V_{DD}.f^2$
c) $P_{avg} = C_{load}^2.V_{DD}^2.f$ d) $P_{avg} = C_{load}.V_{DD}^2.f^2$

6.In constant voltage scaling the doping densities are increased by a factor of

a) S^2 b) S c) 2S d) S^3

7. In terms of MOSFET capacitances the cut-off mode is represented as

a) $C_{gs} = C_{gd} = 0, C_{gb} = C_{ox}.W.L$
b) $C_{gb} = 0, C_{gd} = 0, C_{gs} = \frac{1}{2}C_{ox}.W.L$
c) $C_{gd} = C_{gb} = 0, C_{gs} = \frac{2}{3}C_{ox}.W.L$
d) $C_{gs} = 1,\ C_{gd} = 0, C_{gb} = 1$

8. When power supply voltage is reduced below $V_{TO,n} + |V_{TO,p}|$ the VTC will

a) Follow hysteresis b) Follow sharp VTC
c) Follow practical VTC curve d) Follow no path

9. Condition for Saturation in MOSFET operation is

a) $V_{out} < V_{in} - V_{To}$ b) $V_{out} > V_{in} - V_{To}$
c) $V_{out} > V_{in} + V_{To}$ d) $V_{out} < V_{in} + V_{To}$

10. The condition for surface inversion is

a) $\varphi_s = \varphi_F$ b) $\varphi_s = -\varphi_F$ c) $\varphi_s - \varphi_F = 1$ d) $\varphi_s + \varphi_F = 1$

PART B. (Answer any <u>five</u> of the following question)

Each question carries 4 marks **5×4=20**

1 Explain the Lightly doped drain (LDD) nFET fabrication process?

2. Why Silicon Diode is considered an important material in IC processing. Explain the CVD oxide process with proper diagram?

3.Realise Z=AB+(C+D)(E+F)+GH, using standard CMOS and domino CMOS?

4.Explain Elmore Delay from any RC tree network and take example of any 1 nodes and calculate its delay

5. Explain CMOS Ring Oscillator Circuit?

6.Explain the operating regions of the nMOS and pMOS transistors with the VTC graph of the CMOS inverter?

7.Explain Thermal oxide growth of silicon. What are clean rooms.?

PART C. (Question No 1 is compulsory.
Answer any <u>three</u> questions from the rest)

Question carries 6 marks **6×1 =6**

1.Draw the ckt diagram of the equation $Z = \overline{(D + E + A)(B + C)}$ using CMOS. Draw the layout diagram and stick diagram?