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**SCHOOL OF ENGINEERING AND TECHNOLOGY**

D.C. COURT JUNCTION, DIMAPUR

**End term Examination, DECEMBER 2016**

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| **Course Code:** | EC5T04 | **Semester:** | V | **Total Marks** | 60 |
| **Course Name:** | **Digital System Design** | **Time:** | 3 hrs |

**PART A**

**Answer the following questions (10×1=10)**

1. The keywords for bidirectional switches are \_\_\_\_, \_\_\_\_ and \_\_\_\_.
2. The syntax for sized number specification is \_\_\_\_\_\_\_\_.
3. Using bit reduction operator, ~^4’b1010 = \_\_\_\_\_\_\_\_\_.
4. Logic values used in Verilog are \_\_\_\_\_\_\_.
5. \_\_\_\_\_ triggers the transition in FSM.
6. The output for 4’b0000 && 4’b1101 = \_\_\_\_\_\_.
7. Continuous assignment is used to design sequential logic: True/False.
8. 8’b110000<<2 = \_\_\_\_\_\_\_.
9. Syntax to instantiate CMOS switch is \_\_\_\_\_\_.
10. 8:1 MUX using conditional operator is \_\_\_\_\_\_\_.

**PART B**

**Answer all the questions**

1. Using Mealy state machine, detect the pattern **0100** for i/p sequence x = **11010010011** and o/p ‘z’ if 1-bit overlapping is allowed. **(2)**
2. Write a note on bit-wise operator. **(2)**

**Answer any four (4×4 = 16)**

1. Design a NOR gate using MOS switches and write the Verilog code using switch level modeling.
2. Write a note on the case statement. Also show a 4:1 MUX using case statement.
3. What are sequential UDPs? Explain the level sensitive sequential UDP.
4. Explain in detail the initial statement and always statement.
5. Detect the pattern **1010** for i/p x = **0010101100** and o/p ‘z’ and write the FSM Verilog code using Moore state machine.

**PART C**

**Answer any one (1×6 = 6)**

1. Write the FSM Verilog code for a traffic light controller.
2. Explain in detail blocking and non-blocking assignments.

**Answer any three (3×8 = 24)**

1. Design a random sequence counter 0,1,4,7,2,5 for FSM using

JK-FF.

1. Discuss in detail the timing controls of behavioral modeling.
2. For a function F (A, B, C) = Σ (0, 3, 5, 6, 7), design using multiplexer and write the Verilog code using data flow and structural modeling.
3. Given a sequence of i/p x = **01100001110110** and o/p ‘z’, detect the pattern **0110** using Mealy state machine and design its circuit.

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